LATERAL SUPERJUNCTION SEMICONDUCTOR DEVICE

FIELD OF THE INVENTION

[0001] This invention relates to semiconductor devices and more specifically relates to a novel lateral conduction superjunction MOSFET device.

BACKGROUND OF THE INVENTION

[0002] MOSFET superjunction devices are well known and are disclosed in U.S. Patent 4,754,310 and 5,216,275 and in a publication entitled "Simulated Superior Performance of Semiconductor Superjunction Devices" by Fujihara and Miyaska in the Proceedings of 1998 International Symposium on Semiconductor Devices & ICs, pages 423 to 426. Such superjunction devices have required deep trenches or sequentially deposited and diffused P and N epitaxially layers of silicon. Further, the operational characteristics of prior superjunction devices have not been optimized.

BRIEF DESCRIPTION OF THE INVENTION

[0003] In accordance with a first feature of the invention, a lightly conductive P^{--} substrate is provided, and an N^- epitaxial layer and then a P^- epitaxial layer are grown on the P^{--} substrate. Laterally elongated and spaced trenches are formed from the top of the P^- epitaxial region and extend down and slightly into the N^- substrate. The trenches define P^- mesas between them. An N^- diffusion liner is then diffused into the walls and bottom of the trenches. The trenches are then filled with silicon dioxide insulation. The N^- diffusion liner has a resurf concentration of 1E12 ions per cm^2 over the full exposed N^- trench area. The P^- pillars have a concentration of 2E12 ions/cm^2.

[0004] In other embodiments of the invention, the P^- epi layer can be formed on an SOI (Silicon on Insulator) substrate.

[0005] The novel structure of the invention provides a number of advantages over prior art devices:

1. A shallower trench is needed to fabricate the device. Thus, a 15 micron deep trench can be used in place of a prior art 35 micron trench for a 600 volt device.

2. A denser structure can be made, using a 1 micron pitch. Since pitch is proportional to on-resistance R_{DSON} the reduction of pitch is very desirable.

3. Since the device is a lateral conduction device, it will have a reduced gate charge Q_g which is essential to many applications.

4. The novel structure of the invention lends itself to the integration of plural devices in a common chip, for example, a bridge circuit can be integrated into a single chip.

5. The device can act as a high side switch when the N^{--} layer is designed to support the rail voltage between source and substrate. High side devices, low side devices and control circuitry can then be integrated into the same silicon.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] Figure 1 is a cross-section through a small section of the active area of a wafer after the etching of trenches therein in a process to make a device in accordance with the invention.

[0007] Figure 2 is a cross-section of the area of Figure 1 after the formation of an N^- implant in the trench walls and bottom.

[0008] Figure 3 is a cross-section of Figure 2 after the grooves are filled with oxide.

[0009] Figure 4 is a cross-section like that of Figure 3 after the deposition of oxide over the full upper surface of the active area and is a cross-section of Figure 5 taken across section line 4-4 in Figure 5.

[0010] Figure 5 is a cross-section of Figure 4 taken across section line 5-5 in Figure 4.

[0011] Figure 6 is a top view of the wafer of Figures 4 and 5, showing the main electrode for a plurality of devices integrated into a common chip.

[0012] Figure 7 and Figure 8 are similar to Figures 4 and 5 respectively.

[0013] Figures 9 and 10 show a second embodiment of the invention which eliminates the intermediate N type epi layer of Figures 7 and 8.

[0014] Figures 11 and 12 show a second embodiment of the invention in which an oxide insulation layer is used in place of the N type epi layer of Figures 7 and 8.

DETAILED DESCRIPTION OF THE DRAWINGS

[0015] Referring first to Figure 1, there is shown a small portion of the active area of a wafer 10 of silicon which is to be processed in accordance with the invention. Wafer 10 may have a very lightly doped P^{--} main body 11 of float zone material. A very lightly doped epitaxial layer of N^{--} silicon 12 is grown atop layer 11. P^{-} region 13 is next epitaxially grown atop the N^{--} region 12.

[0016] In one embodiment of the invention, and for a 600 volt device, the P^{-} region 11 may have a concentration of about 2E14 of any desired P type impurity. The N^{--} region 12 may have a concentration corresponding to a dose of 1E12 of a suitable impurity species, thus forming a RESURF dose. The P^{-} region 13 has a concentration corresponding to a double RESURF dose of 2E12 of a suitable P type impurity.

[0017] As further shown in Figure 1, a plurality of parallel laterally elongated trenches 20 to 23 are formed through the P^- region 13 and into the top of N^{--} region 12. The trenches may be of any length, depending on the desired breakdown voltage of the device, and, for a 600 volt device, may be about 40 microns long. The mesa width, that is, the space between trenches, may be about 1.0 microns and the trenches may be about 5 microns deep and about 0.5 microns wide. The trenches preferably extend into N^{--} region 12 for about 0.15 microns. To obtain the desired RESURF dose for the above sized mesa, a P^- concentration of 2E16 ions/cm^3 should be used.

[0018] After forming trenches 20 to 23, and as shown in Figure 2, the walls of the trenches receive an N^- diffusion 30 which produces a RESURF diffusion of equivalent dose of 1E12/cm^2 along the bottoms of the trenches. In order for the structure to work properly, the depth of P^- diffusion 30 and the depth of the trench should be close to one another, and, below the trench, the P concentration should drop to the amount required to support 600 volts (the BV voltage) in the bulk, which is about 2E14 ions per cm^3. One way to achieve this is to control the concentration of the P deposit in the mesas is by diffusion from the sidewalls. The doping could also be achieved by diffusion from a doped film or by bombardment with a doped plasma.

[0019] As next shown in Figure 3, a suitable dielectric, for example, silicon dioxide 35, fills in the trenches by thermal growth or by deposition.

[0020] As next shown in Figures 4 and 5, a MOSgate structure is formed (in any desired sequence) and the source and drain electrodes are also formed. More specifically, the MOSgate structure may include a conventional P^- 40 which contains an N^+ source 41. A P^+ diffusion 42 may also underlie the source region. The center of the source/base structure receives a shallow etch which is later filled by source electrode 43. A conventional gate oxide 44 covers the lateral invertible channel between the source 41 and the lightly doped portion of base 40

regions and a conductive polysilicon gate electrode 50 overlies the gate oxide. An insulation layer 51 of low temperature oxide, for example, insulates gate electrode 50 from the source metal 43.

[0021] As next shown in Figure 5, an N^+ sinker 60 extends from the top of P^- region 13 to N^- diffusion 30 and the N^{--} region 12. The top of regions or mesas 13 receives a field oxide 61 (Figures 4 and 5) which has an opening therethrough to receive drain contact 62 which contacts N^+ sinker 60.

[0022] Figure 6 shows a topology which can be used for the structure of Figures 4 and 5, where a plurality of separate but repeating elements are formed which each laterally adjacent source and drain regions S_1 to S_4 and D_1, D_2 have the same structures as shown in Figures 4 and 5. The source regions S_1 to S_4 may be for separate integrated devices, or alternatively, may be connected together and, similarly, drains D_1 and D_2 may be separate or connected together. Gate electrodes G_1 to G_4 may also be located adjacent sources S_1 to S_4 respectively and are connected to their respective gate electrodes such as gate electrode 50.

[0023] The operation of the device of Figures 4 and 5 is as follows:

[0024] In the blocking mode, and when source 43 and gate 50 are grounded with respect to substrate 12, and a high relative bias is applied to drain 62, the voltage in the lateral direction is supported entirely in the trench structure, and P^- regions 13 and N^- diffusions 30 fully deplete, allowing an almost uniform electric field distribution along the trench length. This depletion region extends downwardly into N^{--}region 12.

[0025] In the conduction mode of operation, and with the application of a bias to gate electrode 50 and the grounding of source 43 relative to substrate 12, an N type channel is formed between source regions 41 and base 40. The application of a bias to drain 60 will cause a current to flow in the device through the undepleted P^- and N^- regions 13 and 30.

[0026] Referring next to Figures 7 to 11, the novel structure of Figures 4 and 5 is duplicated in Figures 7 and 8 so that it can be easily contrasted to the two additional embodiments of Figures 9, 10 and Figures 11 and 12 respectively. The same numerals are used throughout to identify similar components.

[0027] Referring to Figures 9 and 10, there is shown a simplified arrangement compared to that of Figures 4, 5, 7 and 8 which eliminates the N^- region 12 of Figures 7 and 8. Thus, the source 41 and substrate 11 are shorted so the device cannot withstand voltage (preventing its use as a high-side switch). However, the device of Figures 9 and 10 withstands voltage between the drain 60 and the source electrode by the resurf principle.

[0028] Referring next to Figures 11 and 12, an oxide insulation layer 70 is used in place of N^{--} region 12 and the active area is formed on the surface of layer 70. Thus, the device, unlike that of Figures 7 and 8, can be used as a high-side switch.

[0029] Although the present invention has been described in relation to particular embodiments thereof, many other variations and modifications and other uses will become apparent to those skilled in the art. It is preferred, therefore, that the present invention be limited not by the specific disclosure herein, but only by the appended claims.